

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application for:

Possley

Application No.: 09/262,458

Filed: 03/04/1999

Patent No.: 6,974,978 B1

Issued: 12/13/2005

For: GATE ARRAY ARCHITECTURE

Examiner: Ngan V. Ngo

Art Group: 2818

Confirmation No. 9423

Attn: Certificate of Corrections Branch
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR CERTIFICATE OF CORRECTION

Dear Sir:

Upon review of the above-referenced Letters Patent, Applicant noted errors that are the mistake of both the Applicant and the Office. Those errors are as follows:

Fig. 3

Reference numeral 320 appears twice in the drawing. The second appearance of "320" should read --370--.

Insert reference numeral 300 so it applies to the entire flip-flop.

Column 8

Lines 12-15, "... first one or more interconnects interconnecting exclusively first size transistors to form a clock buffer of a logic component, consisting exclusively of first size transistors..." should read ----- first one or more

interconnects interconnecting exclusively first size transistors of one or more adjacent ones of the plurality of arrangements of first size transistors to form a clock buffer of a logic component, consisting exclusively of first size transistors,....

Included with this submission is a Certificate of Correction, which includes a corrected Fig. 3, and it is respectfully requested that a Certificate of Correction be issued. This request for correction is made under the provisions of 37 CFR 1.322 and 1.323.

Payment by Deposit Account No. 500393 is included in the amount of \$100.00 for the fee as set forth in 37 CFR § 1.20(a).

Respectfully submitted,
SCHWABE, WILLIAMSON & WYATT, P.C.

Dated: 10/03/2007

/Aloysius T.C. AuYeung/
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UNITED STATES PATENT AND TRADEMARK OFFICE
CERTIFICATE OF CORRECTION

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PATENT NO. : 6,974,978 B1

APPLICATION NO.: 09/262,458

ISSUE DATE : December 13, 2005

INVENTOR(S) : Possley

It is certified that error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Fig. 3

Reference numeral 320 appears twice in the drawing. The second appearance of "320" should read -370-. Insert reference numeral 300 so it applies to the entire flip-flop.

Column 8

Lines 12-15, "... first one or more interconnects interconnecting exclusively first size transistors to form a clock buffer of a logic component, consisting exclusively of first size transistors..." should read -... first one or more interconnects interconnecting exclusively first size transistors of one or more adjacent ones of the plurality of arrangements of first size transistors to form a clock buffer of a logic component, consisting exclusively of first size transistors,...-.

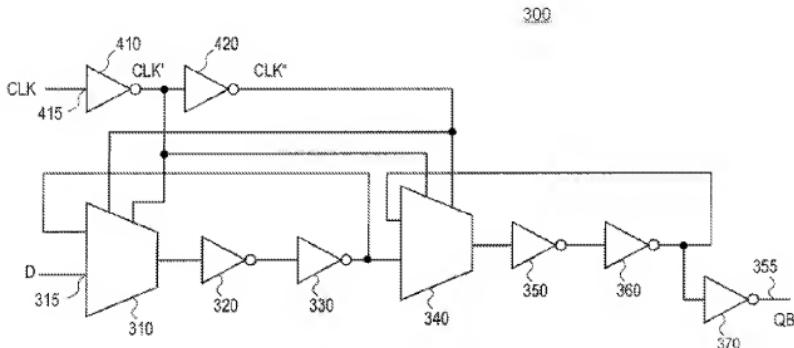


FIG. 3

MAILING ADDRESS OF SENDER (Please do not use customer number below):
SCHWABE, WILLIAMSON & WYATT, P.C., Pacwest Center, Suite 1900, 1211 SW Fifth Avenue, Portland,
Oregon 97204

This collection of information is required by 37 CFR 1.322, 1.323, and 1.324. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 1.0 hour to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Attention Certificate of Corrections Branch, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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